ART FILM - detail1

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 610-60573-01_01.ZIP OR 600-60573-01_01.TGZ.
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
   C. FILL ALL THRU VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005 [.0002] MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

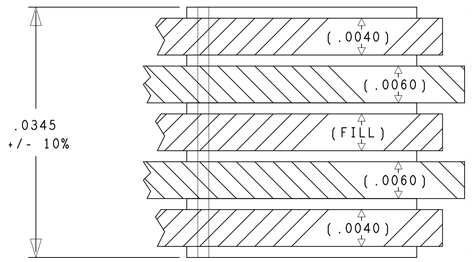
6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

10. EDGE PLATING REQUIRED. COPPER IS EXTENDED PAST THE APPLICABLE EDGES OF THE PCB IN THE PROVIDED DATA TO AID THE EDGE PLATING PROCESS.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF. LAYER	DIFF IMP OHMS	REF. LAYER	DIFF TRACE WIDTH/SPACE
L01 - TOP	0.5 OZ	50	.0188	L03	---	---	.-----/.-----
L02 - PLANE	1.0 OZ	--	-----	---	---	---	.-----/.-----
L03 - SIGNAL	1.0 OZ	--	.-----	---	---	---	.-----/.-----
L04 - PLANE	1.0 OZ	--	.-----	---	---	---	.-----/.-----
L05 - SIGNAL	1.0 OZ	--	-----	---	90	L04/BOT	.0041/.0081
L06 - BOTTOM	0.5 OZ	--	.-----	---	---	---	.-----/.-----

STACK-UP - INCH

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN PLATO	10/14/19
ENGINEER AARA	10/14/19
CHECKER -	-
QA -	-
PROJ. ENG. -	-

CYPRESS EMBEDDED IN TOMORROW
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE
PCB FABRICATION,
CY8CMOD-064B0S2-4343W

SIZE	CAGE CODE	CY P/N
D	-	610-60573-01

SCALE	SHEET	REV
1/1	1 OF 2	01

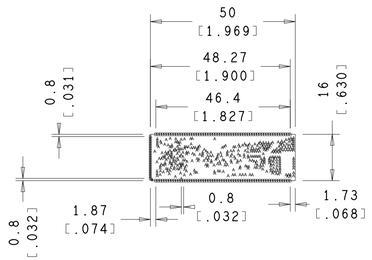
COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60573-01_01.BRD

FAB NOTES REV 04/05/17

ART FILM - detail1

ART FILM - detail2



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN INCHES				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
A	0.0079	+0.0020/-0.0079	PLATED	373
B	0.0158	+0.0020/-0.0118	PLATED	137

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SIZE	CAGE CODE	CY P/N
D	-	610-60573-01
SCALE		SHEET / REV
1/1		2 OF 2 / 01

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60573-01_01.BRD

ART FILM - detail2